Japan Patent Office Industrial Property Digital Library

Japan Patent Office Home Page | Japanese

2003-12-01 Updated

The Industrial Property Digital Library (IPDL) offers the public access to IP Gazettes of the JPO free of charge through the Internet.

Patent&Utility Model

- Patent & Utility Model Gazette DB
- Patent & Utility Model Concordance
- FI/F-term Search
- PAJ
- Patent Map Guidance

Trademark

- Japanese Trademark Database
- Japanese Figure Trademarks
- Japanese Well-Known Trademark
- List of Goods and Services

Database Contents

- Patent & Utility Model Gazette DB
- Patent & Utility Model Concordance
- FI/F-term Search
- PAJ
- Japanese Trademark Database
- Japanese Figure Trademarks

News

News

Link

IPDL Links

Questionnaire

Questionnaire

Notice

Please enable Cookie and JavaScript of the browser when you use the Industrial Property Digital Library.

helpdesk@ipdl.jpo.go.jp

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[The technical field to which invention belongs] Especially this invention relates to the multilayer printed wiring board which has interchange SUTESHARUBAIA hole (IVH) structure, and its manufacture method about a multilayer printed wiring board and its manufacture method.
[0002]
[Description of the Prior Art] The conventional multilayer printed wiring board consists of layered products which accumulate a copper clad laminate and a prepreg by turns, and it comes to unify. This layered product has a front wiring pattern on the front face, and has a inner layer circuit pattern between layer insulation layers. These circuit patterns are electrically connected in the thickness direction of a layered product through the through hole which carried out punching formation between inner layer circuit patterns or between the inner layer circuit pattern and the front wiring pattern.
[0003] However, since the multilayer printed wiring board of through hole structure which was mentioned above needed to secure the field for forming a through hole, it had the fault that the densification of component mounting was difficult and could not fully cope with the request of the microminiaturization of portable electronic equipment, or a ** pitch package and utilization of MCM. Therefore, recently, it replaces with the multilayer printed wiring board of the above through hole structures, and the multilayer printed wiring board which has the interchange SUTESHARUBAIA hole (IVH) structure of being easy to respond to densification attracts attention.
[0004] The multilayer printed wiring board which has this IVH structure is a printed wired board of the structure where the conductive Bahia hall which connects between conductor layers to the insulating layer between each class which constitutes a layered product is prepared. That is, this patchboard is electrically connected by the Bahia hall (a ** Lead Bahia hall or blind BAIA hole) where between inner layer circuit patterns or between a inner layer circuit pattern and a front wiring pattern do not penetrate a wiring substrate. So, the multilayer printed wiring board of IVH structure does not need to prepare the field for forming a through hole specially, and can realize miniaturization of electronic equipment, and densification easily.
[0005] The multilayer printed wiring board of such IVH structure is manufactured according to distance as shown in drawing 7 . First, using the material which infiltrated the epoxy resin into aramid non-**** as a prepreg 112, the perforating process by the carbon dioxide laser is performed to this prepreg 112, and hole part 112a subsequently obtained by doing in this way is filled up with the conductive paste 114 (refer to drawing 7 (A)).
[0006] Next, copper foil 116 is put on both sides of the above-mentioned prepreg 112, and it

heats and pressurizes with a heat press. Thereby, the epoxy resin and the conductive paste of a prepreg 112 are hardened, and the double-sided steel foil 116 and electrical installation between 116 are performed (refer to drawing 7 (B)).

[0007] And the hard double-sided substrate which has the Bahia hall is obtained by carrying out patterning of the above-mentioned copper foil 116 by the etching method (refer to drawing 7 (C)). Thus, the obtained double-sided substrate is multilayered as a core layer. After carrying out a laminating one by one and carrying out a heat press again, specifically carrying out alignment of the prepreg and copper foil which filled up both sides of the above-mentioned core layer with the above-mentioned conductive paste, a four-layer substrate is obtained by **********ing the copper foil 116 of the best layer (refer to drawing 7 (D) and (E)). When multilayering furthermore, it carries out by repeating the above-mentioned process, and considers as six layers and an eight-layer substrate.

[0008]

[Problem(s) to be Solved by the Invention] However, the conventional technology mentioned above is that must repeat repeatedly heating by the heat press, a pressurization process, and the patterning process of the copper foil by etching, a manufacturing process becomes complicated, and manufacture takes a long time. And since it is difficult for the multilayer printed wiring board of the IVH structure acquired by such manufacture method to check poor patterning of copper foil in manufacture process, if aforementioned poor patterning generates in manufacture process (at least one process [one]), the whole patchboard which is a final product will serve as a defective.

[0009] That is, when at least one defective was taken out among each laminating process, the above-mentioned conventional manufacture process had to be disposed of to the thing of other good laminating processes, and had the fatal fault of being easy to cause aggravation of manufacture efficiency or the manufacture yield.

[0010] The place which it is made in order that this invention may solve the technical problem mentioned above, and is made into the purpose is to offer the multilayer printed wiring board and its manufacture method of the IVH structure which can be efficiently manufactured by the high yield.

[0011]

[Means for Solving the Problem] Since the above-mentioned purpose is attained, this invention can be constituted as follows.

** The process which forms the hole which results in this metal layer in the insulating base material by which the metal layer was formed in one field in a laser beam, The process which fills up with a metal the hole formed by ****, and forms the Bahia hall, ** a metal layer -- **********ing -- a conductor -- the process and ** Bahia hall front face which form a circuit -- the letter of a salient -- the process which forms a conductor and is made into the one side circuit board -- ** Carry out the laminating of the circuit (you may be the one side circuit board) through an anisotropy electric conduction film. the letter of a salient of the one side circuit board -- a conductor and the conductor of other substrates -- heating pressurization -- carrying out -- the letter of a salient -- a conductor is pressed on an anisotropy electric conduction film -- making -- the Bahia hall -- this anisotropy electric conduction film -- minding -- a conductor -- while making it connect with a circuit -- this one side circuit board -- being concerned -- others -- the process which unifies a substrate

[0012] Moreover, since the above-mentioned purpose is attained, this invention can be constituted as follows.

** the process which forms the hole which results in this metal layer in the insulating base material by which the metal layer was formed in one field in a laser beam, the process which form the Bahia hall which fills up with a metal the hole formed by ****, and has a salient, and

a ** metal layer -- **********ing -- a conductor -- the conductor of the salient of a process and ** one side circuit board which forms a circuit and makes into the one side circuit board, and other substrates -- a circuit (it may be the one side
a laminating is carried out through a ******** electric conduction film, heating pressurization is carried out and this salient is pressed on an anisotropy electric conduction film -- making -- the aforementioned Bahia hall -- this anisotropy electric conduction film -- minding -- a conductor -- while making it connect with a circuit -- this one side circuit board -- being concerned -- others -- the process which unifies a substrate
[0013] the conductor which formed the predetermined circuit pattern according to the multilayer printed wiring board and its manufacture method of this invention -- the one side circuit board which has a circuit is manufactured separately beforehand before [for this reason,] carrying out the laminating of this one side circuit board -- a conductor -- since the existence of the poor part of a circuit etc. can be inspected, in a laminating stage, it becomes possible to use only the poor one side circuit board which is not That is, in the manufacture method of this invention, poor generating in a manufacture stage decreases and the multilayer printed wiring board of IVH structure can be manufactured by the high yield.
[0014] Moreover, the manufacture method of the multilayer printed wiring board of this invention does not need to repeat a heat press, accumulating a prepreg like the conventional technology. That is, in this invention, the heat press of two or more one side circuit boards can be carried out at a time in piles through the anisotropy electric conduction film arranged in this one side circuit board. For this reason, it is not necessary to repeat a complicated heat press distance, and the multilayer printed wiring board of IVH structure can be efficiently manufactured by the manufacture method of this invention in a short time. Furthermore, since it is unifying by the physical force with one press, it excels also in connection reliability.
[0015] In addition, it is desirable to perform drilling of the hole for the Bahia halls to an insulating substrate with laser by the manufacture method of this invention. When carrying out densification of the multilayer printed wiring board, as for the Bahia hall of the one side circuit board, it is advantageous for it to be detailed and highly precise and to form, and this is because it is easily highly precise and a detailed hole can be formed with laser.
[0016]
[Embodiments of the Invention] The multilayer printed wiring board applied to the embodiment of this invention below and its manufacture method are explained with reference to drawing. Drawing 1 shows the longitudinal section of the multilayer printed wiring board which takes like the 1st operative condition as for this invention. A multilayer printed wiring board 10 is a laminated circuit board which consists of the arranged one side circuit boards 30A, 30B, 30C, and 30D two-layer [every] on the upper surface and the inferior surface of tongue of the core substrate 20 arranged in the center, and this core substrate 20.
[0017] the conductor of a pattern predetermined to one field of these one side circuit boards 30A, 30B, 30C, and 30D -- Circuits 32a, 32b, 32c, and 32d are formed, and the anisotropy electric conduction films 34A, 34B, 34C, and 34D are arranged in the field of another side The core substrate 20 and the one side circuit boards 30A, 30B, 30C, and 30D have pasted up through these anisotropy electric conduction films 34A, 34B, 34C, and 34D. The blind BAIA holes 36a, 36b, 36c, and 36d where it filled up with the conductive metal paste are formed in each one side circuit boards 30A, 30B, 30C, and 30D, and the bumps 38a, 38b, 38c, and 38d who consist of a pewter are formed in the upper part of this Bahia hall.
[0018] namely, the multilayer printed wiring board 10 -- setting -- the conductor of one side circuit board 30A of the lowest layer -- circuit 32a is connected to bump 38a through Bahia hall 36a this bump 38a -- anisotropy electric conduction film 34A on top -- pressing -- **** -- this anisotropy electric conduction film 34A -- minding -- the conductor of one side circuit

board 30B -- it connects with circuit 32b this -- a conductor -- bump 38b connected through circuit 32b and Bahia hall 36b minds with anisotropy electric conduction film 34B on top, and the flow with the through hole 24 of the core substrate 20 is taken The through hole 24 of this core substrate 20 is connected with bump 38c through anisotropy electric conduction film 34of one side circuit board 30C by the side of the upper surface C. the conductor connected through this bump 38c and Bahia hall 36c -- circuit 32c is connected with bump 38d through anisotropy electric conduction film 34of one side circuit board 30D of best side D this bump 38d -- Bahia hall 36d -- minding -- a conductor -- it connects with 32d of circuits IC package 12 and a bare chip 16 arrange in one side circuit board 30D of this best side -- having -- the conductor of this one side circuit board 30D -- it connects with Circuits 32d and 32d through the pewter 14 thus, the conductor of one side circuit board 30A of the lowest layer of a multilayer printed wiring board -- the conductor of circuit 32a and one side circuit board 30D of the best layer -- the chips 12 and 16 on a circuit 32 are connected through the blind BAIA holes 36a, 36b, 36c, and 36d These Bahia hall constitutes an interchange SUTESHARUBAIA hole.

[0019] Then, the manufacture method of this multilayer printed wiring board 10 is explained. Here, the manufacture method of the core substrate 20 is first described with reference to drawing 2 . As shown in the distance (A) of drawing 2 , let pasting ********** be start material for copper foil 21 at both sides of the substrate 22 made of BT (BISUMAREIDOMIDO triazine) resin. As shown in distance (B), after drilling hole 22a for through holes in this substrate 22, a through hole 24 is formed by performing electroless-plating processing and giving copper plating in this hole 22a. a conductor predetermined by performing etching processing and removing the garbage of copper foil 21, after applying the etching resist which is not illustrated beforehand, as shown in distance (C) -- a circuit 25 is formed it is shown in distance (D) -- as -- this -- a conductor -- melanism-reduction processing is performed and roughened on a circuit 25 and the front face of a through hole 24 the this restoration resin as shown in distance (E), after applying the restoration resin 26 uniformly by the roll coater and stiffening this restoration resin -- a belt sander etc. -- a conductor -- it grinds until a circuit 25 is exposed to a front face, and both sides manufacture the flat core substrate 20

[0020] this core substrate 20 -- the interior of a through hole 24, and a conductor -- side 25a of a circuit 25 roughens -- having -- a conductor -- the adhesive property of a circuit 25 and the restoration resin 26 is improved for this reason -- this -- a conductor -- it can prevent that a crack occurs with the anisotropy electric conduction film 34 mentioned above with reference to drawing 1 with the interface of a circuit 25 and the restoration resin 26 as the starting point

[0021] Then, with reference to drawing 3 and drawing 4 , the manufacture method of the one side circuit board 30 is explained. As shown in the distance (A) of drawing 3 , let the insulating base material 40 by which the metal layer 42 was formed in one side be start material. Here, as an insulating base material 40 to be used, it is desirable that it is one sort chosen from films, such as glass epoxy-group material, an aramid fiber-polyimide base material, a bismaleimide triazine resin base material, a polyphenylene-ether (PPE) film, and a polyimide (PI).

[0022] Moreover, copper foil, a nickel foil, aluminum foil, etc. can be used for the metal layer 42 formed in the insulating base material 40. Mat processing of the copper foil may be carried out for the adhesion improvement. Here, it is most advantageous in cost to use an one side copper clad laminate. The thickness of the insulating base material 40 has good 40-60 micrometers. It is for securing insulation. On the other hand, the thickness of the metal layer 42 has good 12-18 micrometers. this mentions later -- as -- laser -- a hole -- if it is because it will penetrate if too thin, in case dawn is carried out and is too thick conversely -- etching --

the bottom -- the time -- a conductor -- it is because it is hard to form a circuit
[0023] subsequently, laser -- the resin insulation base material 40 -- a hole -- 40a is opened (distance (B)) A carbon dioxide laser, UV laser, an excimer laser, etc. can be used for laser. Moreover, 50-150 micrometers of an aperture are good. The carbon dioxide laser is most suitable for using cheaply and industrially, and is the most desirable laser to the invention in this application. Here, when a carbon dioxide laser is used, in order that the resin slightly fused on the front face of the metal layer 42 may remain, it is desirable [it is in this hole 40a, and] to perform DESUMIA processing.
[0024] then, the hole opened by laser -- 40a is filled up with a metal 46 and it is referred to as Bahia hall 36a (distance (E)) Here, restoration of a metal 46 is filled up with a conductive paste, or electrolysis plating performs it. A conductive paste can use at least one sort chosen from silver, copper, and a golden paste. Since it is difficult, the electrolysis plating of on the other hand the bottom of drilling of the diameter of detailed of 50 micrometers or less of apertures filling up a metal paste with laser is more practical.
[0025] When filled up with electrolysis plating, electrolysis plating is performed by considering the metal layer 42 formed in the insulating base material 40 as a plating lead. here -- before electrolysis plating -- a hole -- it is good to carry out activation of the front face of the metal layer 42 in 40a from an acid etc. In case it galvanizes, as the mask 48 is covered over the metal layer 42 side, or are shown in distance (D), and are shown in distance (C) and the same insulating base material 40 cannot be touched [laminating adhesion of two sheets and the metal layer 42 comrades is carried out and] at plating liquid, electrolysis plating is performed so that electrolysis plating may not deposit in the front-face side of the metal layer 42 formed in the insulating base material 40.
[0026] The plating film (metal 46) which rose from hole 40a as shown in the distance (F) of drawing 4 is removed by polish etc. after electrolysis plating. Polish can use a belt sander, buff ****, etc.
[0027] it is shown in distance (G) -- as -- the metal layer 42 -- **********ing -- a conductor -- as pretreatment for forming a circuit, first, the metal layer 42 whole is **********ed and thickness is made thin to about 1 - 5 micrometers This becomes easy to form a pattern. the metal layer 42 as shown in distance (H), after covering the mask of a predetermined pattern -- **********ing -- a conductor -- circuit 32a is formed Here, first, a dry film is stuck, and along with a predetermined circuit pattern, exposure and after carrying out a development and forming an etching resist, an etching-resist agenesis portion is **********ed. At least one sort of etching chosen from the solution of a sulfuric-acid-hydrogen peroxide, a persulfate, a cupric chloride, and a ferric chloride is good.
[0028] in addition, a conductor -- as for the front face of circuit 32a, it is desirable to carry out roughening processing It is for improving adhesion with the anisotropy electric conduction film 34 mentioned above with reference to drawing 1 , and preventing generating and exfoliation of a crack. Roughening processing has good surface roughening by the etching reagent tradename [formation of the needlelike alloy plating (tradename interchange plate made from the Ebara you gymnite) which consists of melanism (oxidization)-reduction processing or copper-nickel-Lynn, and / made from MEKKU] "MEKKU dirty bond" becoming.
[0029] next, distance (I) -- a conductor -- the field in which circuit 32a was formed -- an opposite side -- it is -- the front face of Bahia hall 36a -- the letter of a salient -- a conductor (bump) -- 38a is formed the letter of a salient -- a conductor -- 38a is formed by screen-stenciling using the metal mask with which the conductive (pewter) paste was prepared in opening in the predetermined position, or performing solder plating
[0030] this state -- a conductor -- whether there is any faulty connection in circuit 32a and bump 38a, and a conductor -- it inspects whether the insulation between circuit 32a can be

taken if a laminating is carried out in the multilayer printed wiring board of the conventional technology and it is not after completion, as mentioned above -- a conductor -- since the existence of a poor part can be inspected before carrying out the laminating of the one side circuit board 30A in this embodiment to the ability to have not inspected a circuit, in the laminating stage mentioned later, only poor one side circuit board 30A which is not is used -- things are made

[0031] finally, it is shown in distance (J) -- as -- the letter of a salient of this insulating base material 40 -- a conductor (bump) -- the 38a side front face or a conductor -- non-hardened anisotropy electric conduction film 34A is laminated on circuits 32b and 25 and the 32c side front face especially -- a conductor -- the case where a roughening layer is formed in Circuits 32b, 25, and 32c -- a conductor -- it is better to laminate in circuit self The thickness of an anisotropy electric conduction film is 10-50 micrometers. It is desirable.

[0032] then, the laminating distance of the core substrate 20 come out of and mentioned above with reference to drawing 2 and the one side circuit board 30 mentioned above with reference to drawing 3 and drawing 4 is explained with reference to drawing 5 As shown in distance (K), this one side circuit board 30A, the one side circuit boards 30B, 30C, and 30D formed in the same distance with having mentioned above, and the core substrate 20 are piled up. Here, that with which inspection of a poor part was able to be managed is used for all the one side circuit boards 30A, 30B, 30C, and 30D and core substrates 20. First, one side circuit board 30B is laid on anisotropy electric conduction film 34of one side circuit board 30A A, and the core substrate 20 is laid again on anisotropy electric conduction film 34of this one side circuit board 30B B. Here, on this core substrate, reversal, i.e., anisotropy electric conduction film 34of one side circuit board 30C C, piles up the one side circuit boards 30C and 30D so that anisotropy electric conduction film 34of one side circuit board 30D D may turn to this one side circuit board 30C side toward this core substrate 20 side. This superposition is performed carrying out alignment of the guide holes (not shown) prepared in the circumference of the one side circuit board 30 and the core substrate 20 by inserting in a guide pin (not shown). Here, the portion of the cycle C in drawing of the substrate by which the laminating was carried out is expanded, and it is shown as (M).

[0033] The substrate finally piled up as shown in distance (L) is heated at 150-180 degrees C using a heat press, and it is 20 - 50 kgf/cm2. By pressurizing, each one side circuit boards 30A, 30B, 30C, and 30D are unified in the shape of a multilayer by one press forming. The portion of the cycle C in drawing of the substrate by which the laminating was carried out is expanded, and it is shown as (N). being pressurized first here -- bump 38a of this one side circuit board 30A -- the conductor by the side of this bump 38a and one side circuit board 30B -- anisotropy electric conduction film 34A which intervenes between circuit 32b is pressed, and only this press portion is made into conductivity, maintaining the insulation of other portions thereby -- this bump 38a and a conductor -- the electric connection with circuit 32b is taken the same -- other Bumps 38b, 38c, and 38d (refer to drawing 1) and anisotropy electric conduction films 34B, 34C, and 34D of the one side circuit boards 30B, 30C, and 30D -- minding -- a conductor -- connection with a circuit is taken Furthermore, by being heated simultaneously with pressurization, the anisotropy electric conduction film 34 of one side circuit board 30A hardens, and firm adhesion is performed between one side circuit board 30B. In addition, as a heat press, it is suitable to use a vacuum heat press. The multilayer printed wiring board 10 which this mentioned above with reference to drawing 1 is completed.

[0034] Then, this invention sticks like the 2nd operative condition, and it explains with reference to drawing 6 . the distance (E) shown in drawing 3 in the embodiment mentioned above -- a hole -- after filling up 40a with a metal 46, the plating film (metal 46) which rose from hole 40a as shown in the distance (F) of drawing 4 was ground and removed On the

other hand, it sets like the 2nd operative condition and the height to which this Bahia hall 36a rose is used as it is.
[0035] first, the conductor of one side circuit board 30B which serves as the upper layer of one side circuit board 30A like the distance (A) shown in drawing 6 -- anisotropy electric conduction film 34A is laminated like the 1st embodiment on circuit 32b Then, as shown in distance (B), the one side circuit boards 30A, 30B, 30C, and 30D and the core substrate 20 are piled up. The substrate finally piled up as shown in distance (C) is heated at 150-180 degrees C using a heat press, and it is 20 - 50 kgf/cm2. By pressurizing, each one side circuit boards 30A, 30B, 30C, and 30D are unified in the shape of a multilayer. being pressurized first here -- the height 37 of the Bahia hall a of this one side circuit board 30A -- this height 37 and the conductor by the side of one side circuit board 30B -- anisotropy electric conduction film 34A which intervenes between circuit 32b is pressed, and only this press portion is made into conductivity, maintaining the insulation of other portions thereby -- the height 37 of this Bahia hall 36a, and a conductor -- the electric connection with circuit 32b is taken the same -- other height 37 and anisotropy electric conduction films 34B, 34C, and 34D of the one side circuit boards 30B, 30C, and 30D -- minding -- a conductor -- connection with a circuit is taken Furthermore, by being heated simultaneously with pressurization, the anisotropy electric conduction film 34 of one side circuit board 30A hardens, and firm adhesion is performed between one side circuit board 30B. Thereby, a multilayer printed wiring board [like] is completed the 2nd operative condition.
[0036] The manufacture method [like] has this advantage that can cut down distance compared with the 1st embodiment the 2nd operative condition. On the other hand, the 1st operative condition, after it smooths the front face of the Bahia hall, in order that it may form a bump, a method [like] tends to keep this bump's height constant, is applying the uniform force to the anisotropy electric conduction film 34, and has the advantage which cannot generate a faulty connection easily.
[0037] Although the embodiment mentioned above explained the multilayer printed wiring board which the one side circuit board 30 of four layers piled up, the composition of this invention is applicable also to the multilayer printed wiring board of three layers or five layers or more. Furthermore, the laminating of the one side circuit board of this invention can be carried out to the one side printed circuit board created by the method of the conventional technology, a double printed board, a double-sided through hole printed circuit board, and a multilayer printed board, and a multilayer printed wiring board can also be manufactured.
[0038] Moreover, although the hole for forming the Bahia hall was formed in the embodiment mentioned above using laser, it is also possible to perforate by the mechanical methods, such as drilling and punching processing.
[0039] Furthermore, the one side circuit board which constitutes the multilayer printed wiring board of this invention has pasted up with other one side circuit boards and the core substrate through the anisotropy electric conduction film. As a substrate which pastes up the one side circuit board, the various printed-circuit boards known from the former can be used.
[0040] moreover, various processing processings, for example, formation of a solder resist on a front face, in which the multilayer printed wiring board of this invention is generally performed to a printed wired board and a surface conductor -- the nickel/gilding to a circuit, pewter processing, a perforating process, mold cavity processing, through hole plating processing, etc. can be performed
[0041]
[Effect of the Invention] as mentioned above, the conductor which formed the predetermined circuit pattern according to this invention -- the one side circuit board which has a circuit is manufactured separately beforehand before [for this reason,] carrying out the laminating of

this one side circuit board -- a conductor -- a laminating stage enables it to use only the poor one side·circuit board which is not by inspecting the existence of the poor part of a circuit etc. That is, in the manufacture method of this invention, poor generating in a manufacture stage decreases and the multilayer printed wiring board of IVH structure can be manufactured by the high yield.

[0042] Moreover, the manufacture method of the multilayer printed wiring board of this invention does not need to repeat a heat press, accumulating a prepreg like the conventional technology. That is, in this invention, the heat press of two or more one side circuit boards can be carried out at a time in piles through the anisotropy electric conduction film arranged in this one side circuit board. For this reason, it is not necessary to repeat a complicated heat press distance, and the multilayer printed wiring board of IVH structure can be efficiently manufactured by the manufacture method of this invention in a short time. Furthermore, since it is unifying by the physical force with one press, it excels also in connection reliability.

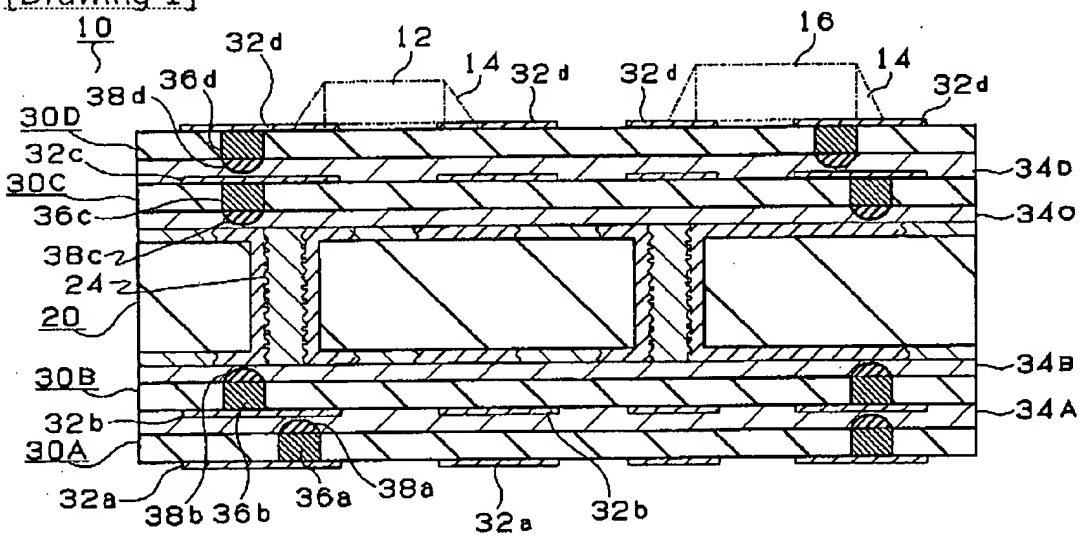
[Translation done.]

* NOTICES *

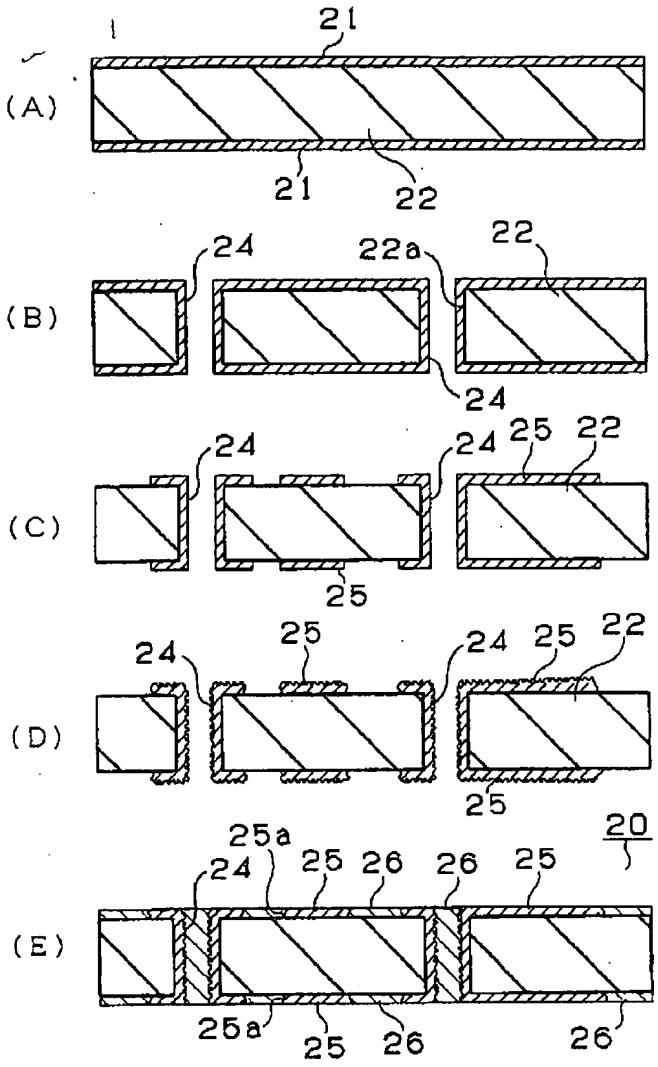
1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DRAWINGS

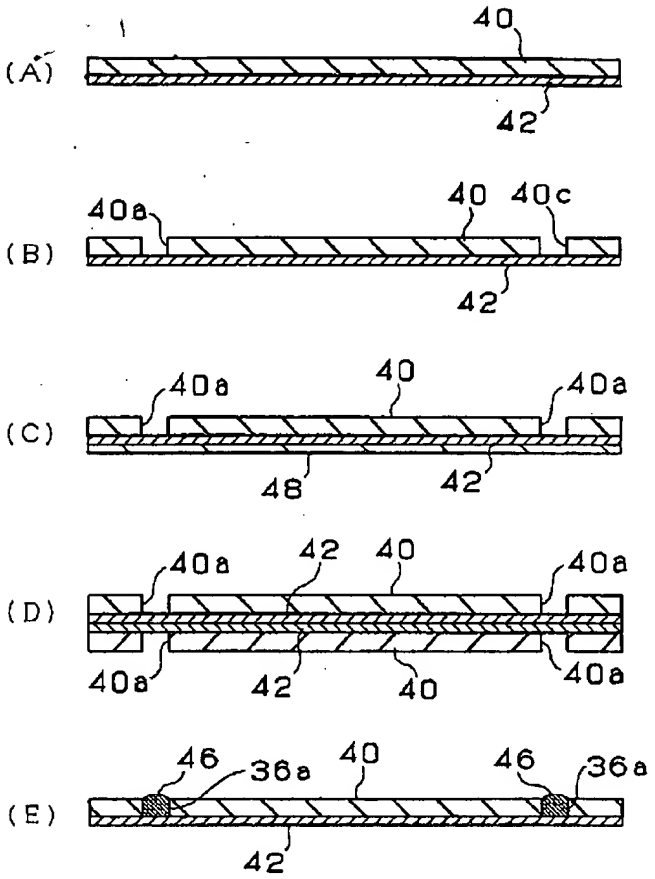
[Drawing 1]



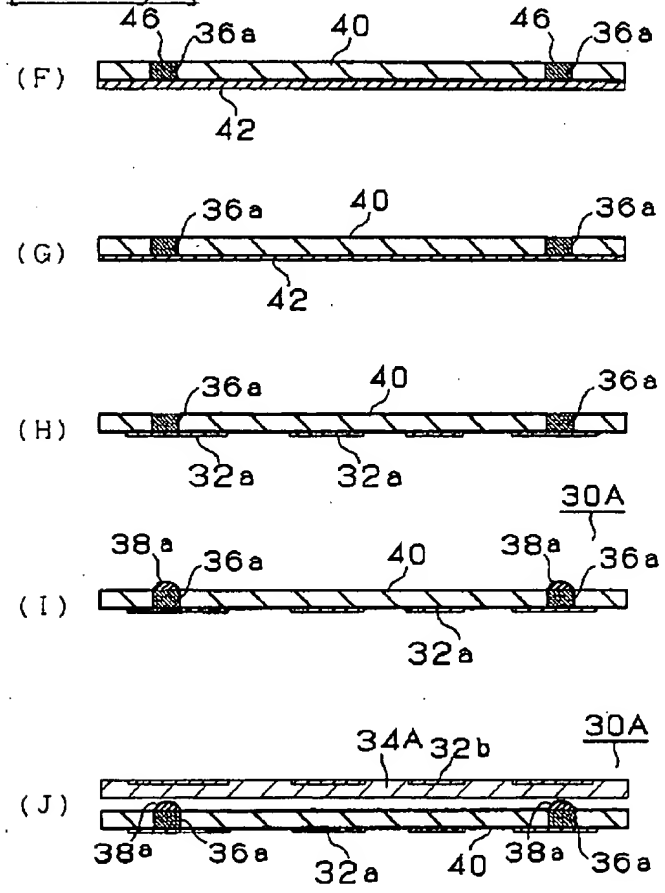
[Drawing 2]


(A)
21
21
22
(B)
24
22a
22
24
(C)
24
24
25
22
25
(D)
24
25
24
25
22
25
(E)
20
25a
24
25
26
26
25
25a
25
26
26

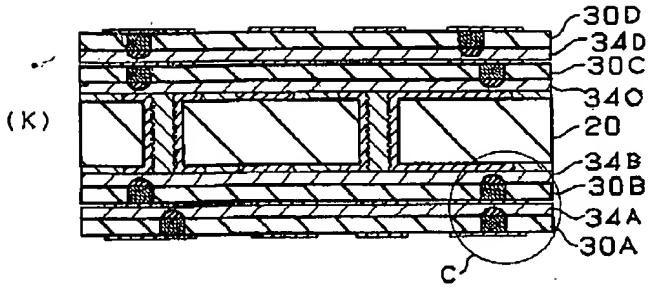
[Drawing 3]

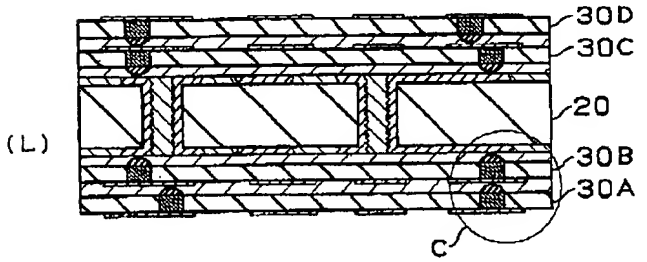


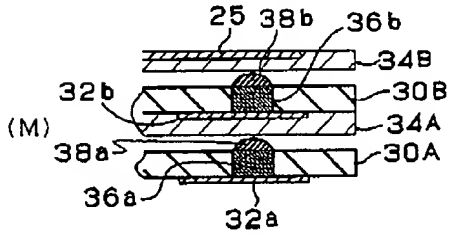
[Drawing 4]

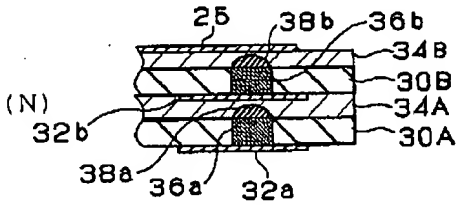


[Drawing 5]

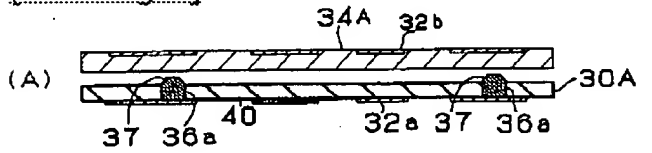

(K)
30D
34D
30C
34C
20
34B
30B
34A
30A
C

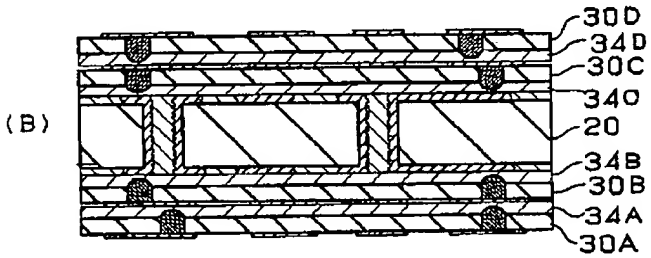

(L)
30D
30C
20
30B
30A
C

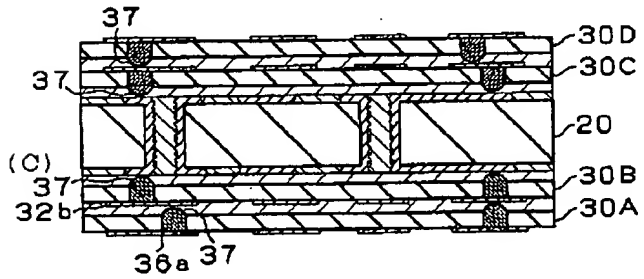

(M)
25
38b
36b
34B
32b
30B
34A
38a
30A
36a
32a


(N)
25
38b
36b
34B
30B
34A
32b
30A
38a
36a
32a

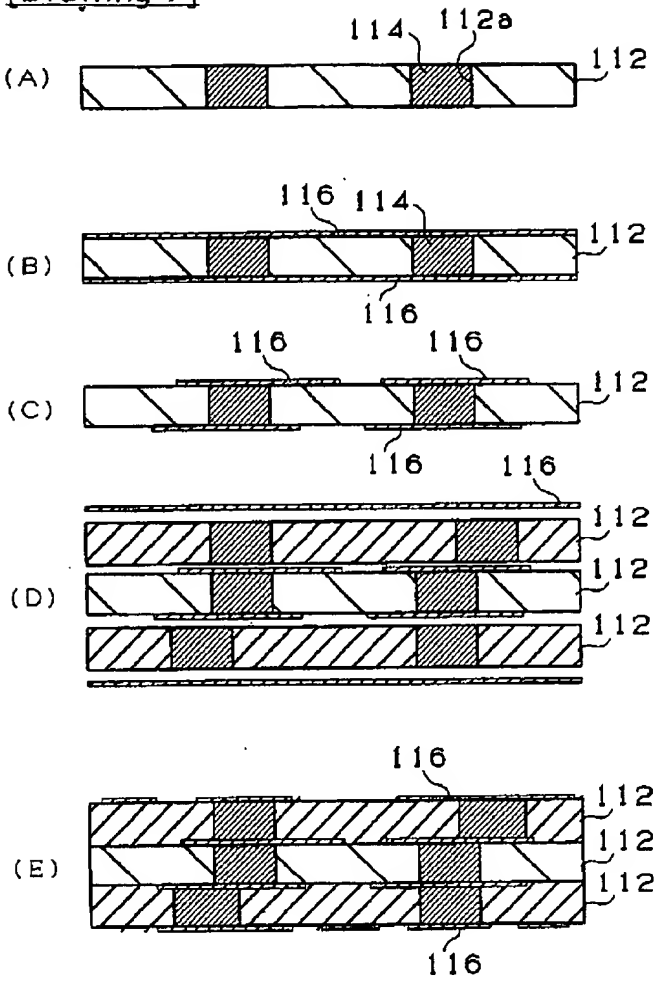
[Drawing 6]


(A)
34A
32b
30A
37
36a
40
32a
37
36a


(B)
30D
34D
30C
34C
20
34B
30B
34A
30A


37
37
(C)
37
32b
36a
37
30D
30C
20
30B
30A

[Drawing 7]



[Translation done.]